ANALOG DEVICES

CPL

ICs FOR LASERS

USING THE AD9660 EVALUATION BOARD

Introduction

The AD9660 evaluation board is comprised of two printed circuit boards. The Laser Diode Driver (LDD) Resource board is both a digital pattern generator and an analog reference generator (see LDD Resource Board Block Diagram). The board is controlled by an IBM compatible personal computer through a standard printer cable. The resource board interfaces to the AD9660 DUT board, which contains the AD9660, level shift circuits for the analog inputs, and a socket for an R type laser diode. A dummy load circuit for the laser diode is included for evaluation. Power for all the boards is provided through the banana jacks on the AD9660 DUT board. These should be connected to a linear, +5V power supply. Schematics for the LDD Resource board, AD9660 DUT, and Dummy Load are included, along with a bill of material and layout information.

Plugging the boards together

The LDD Resource board and AD9660 DUT board are normally plugged together for shipment. If they become separated for any reason, the user may plug them together. The LDD Resource board sits on top of the AD9660 DUT board; line up the 20 pin headers. Five SMB connectors also plug together once the 20 pin headers are aligned. It is best to have power supplies off during this operation.

PC Requirements

The AD9660 evaluation board requires an IBM compatible personal computer with the following:

1. Windows version 3.1 software.
2. Standard parallel printer port.
3. A Mouse.

The printer cable should be removed from any printer (or other device) and plugged into the Centronics connector on the LDD Resource board (P1) before running any software for the board. The control software will use the LPT1 printer port address by default. To change the address, click the "Change Port Address" button with the mouse and select the appropriate address.

** **Warning** ** Some printer cables may not have all 25 pins connected to the centronics connector. Such cables should not be used for controlling the LDD Resource board.

Software Control

The LDD Resource board is controlled through a standard printer cable. Installation of the software is simple. Insert the 3.5" diskette labeled "AD9660 Demo Software" into the PC's floppy disk drive. From the Windows File Manager choose FILE / RUN. In the command line type "B:\SETUP" (assuming the floppy drive is drive B). The software will install the control software on the computer's hard drive, and place a Group called "AD9660", and an icon called "AD9660" in Program Manager.

NOTE: The installation software assumes there is a file called vbrun300.dll in the windows \SYSTEM directory. If there is not, the installation software will generate an error message and terminate. If this occurs, copy the file from the "AD9660 Demo Software" floppy into the windows \system directory. The software should then install properly.

Once the software is installed on the hard drive, double click the AD9660 icon to start the control software. The LDD Resource boards and the AD9660 DUT board should be attached to the PC's printer cable and the power supply to the AD9660 DUT (+5V) active before the software is initiated. When the software is running, all commands are mouse driven.

The analog reference circuit on the LDD Resource Board provides two buffered 8 bit DAC's. The two references are controlled with the SLIDE controls marked "Bias DAC" and "Write DAC", and vary from 0 to 2.55V. These in turn are level shifted on the AD9660 DUT board so that the BIAS LEVEL and WRITE LEVEL inputs are between V_{REF} and V_{REF} + 1.6V. When the software is initiated, the Bias and Write DAC levels are set to 0V. Once a pattern is enabled (see below) the Bias DAC is set to 10%, and the Write DAC level is set to 20%. The user may adjust levels at any time after the software is running.

The digital pattern generator copies patterns (from files named *.pat) into the 32Kx16 SRAM memory, and reads them out to the DUT board's interface for the AD9660's DISABLE, BIAS CAL, WRITE CAL, WRITE PULSE, and OFFSET PULSE pin connections. The WRITE PULSE pattern's pulse width is modulated

on the LDD Resource by the AD9560. Contact Application Engineering for more information.

The pattern generator can store patterns of up to 800μs with the on board 40MHz clock providing 25ns intervals. All signals have a minimum pulse width of 25ns (one clock period), except WRITE PULSE, whose pulse width is controlled by the AD9560, and may be as low as 2ns.

Five standard patterns are shipped with the software for evaluation. They are:

1. MOD50.PAT
2. MODMIX.PAT
3. PCAL30.PAT
4. PCAL20.PAT
5. BIASCAL.PAT

BIASCAL.pat is a static pattern with BIASCAL HIGH, and all other control signals LOW. It is intended to allow the user to measure output power from a laser diode, or to adjust the feedback resistor of the AD9660 (see below). All other patterns are dynamic, and are documented on pages 7-10. Loading the patterns is done by clicking the mouse on one of the file names in the "PATTERN SELECTION MENU". This will bring up a new dialog box prompting the user to verify the selection. This list will contain the 5 patterns discussed above, along with any custom patterns added to the software. Custom patterns should be requested through Applications engineering, and are generally generated within 24 hours of a request.

Once a pattern is selected, the software will load the SRAM; this may take several minutes depending on the size of the pattern and speed of the PC. The software will also verify the pattern to detect errors, if errors cannot be corrected by the software, a message box will prompt the user to contact Applications Engineering. The user should check that the port address is correct, the printer cable is connected, and that the power supply is on as these are the most frequent problems in loading patterns.

NOTE: The length of the printer cable can cause problems while loading patterns, a cable no longer than 6 ft is recommended.

When the control software is first run, the LDD Resource board keeps the control signals in a safe state:

DISABLE = HIGH
WRITE PULSE = LOW
WRITE CAL = LOW
OFFSET PULSE = LOW
BIAS CAL = LOW

This state remains until a pattern is loaded and initiated by the user clicking the mouse in the "ON" button. The pattern stored in memory is repeated until the user clicks the mouse in the "OFF" button, when the control signals are returned to the safe state.

Laser Safe State

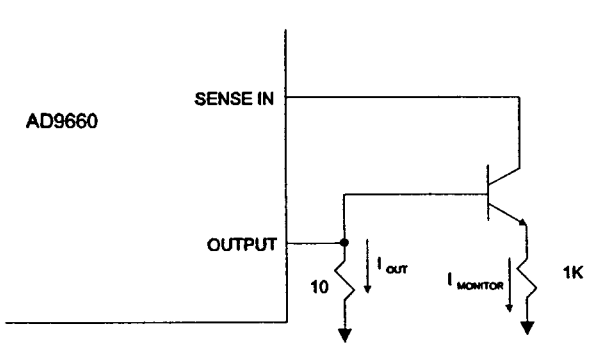
The user may disable the pattern generator to the safe state described above, and return the Bias DAC level to 10% and the write DAC level to 20% by clicking the mouse on the "LASER OFF" button.

Adjusting the AD9660's Feedback resistor, R_{GAIN}

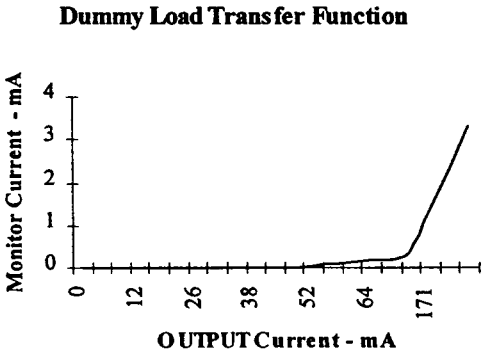
R_{GAIN} is set by adjusting R3 on the AD9660 DUT board. R3 is a 470Ω surface mount, 1 turn potentiometer. Adjustment of R3 adjusts the total feedback of the transimpedance amplifier from 300 to 985Ω. R_{GAIN} should be adjusted to match the laser diodes monitor current. Alternatively, Rgain can be set to a fixed value by removing R2, R3, C2, and then installing the appropriate values for R1 and C1. Contact Applications Engineering for additional information.

AC performance characterization

Once the software is running, the user may observe the ac switching characteristics of the AD9660 by probing the output directly when using the dummy load circuit. The TRIGGER output (J2) of the LDD Resource board is helpful in triggering the waveform on an oscilloscope. Laser performance can be characterized by replacing the dummy load with an R type laser, and capturing the laser's light output with a fast external photodiode. Contact applications engineering for more information.



AD9660 DUMMY LOAD CIRCUIT



Connecting other control signals

The AD9660 DUT board may be unplugged from the LDD Resource board and used independently. SMB cables and ribbon cables are available from applications engineering. Users should review the schematics of the AD9660 DUT board and the AD9660 preliminary data sheet before interfacing the board to other control signals.

"ABOUT AD9660"

Slecting the "ABOUT AD9660" button will bring up a window with applications information (how to contact Applications Engineering , etc) and a pinout of the AD9660.

Contacting Applications Engineering

Applications Information is gladly provided by contacting the following:

David Buchanan

email:
DAVID.BUCHANAN@ANALOG.COM

Phone: 910 - 605 - 4252

Fax: 910 - 668 - 0101

or

David Tesh

email:
DAVID.TESH@ANALOG.COM

Phone: 910 - 605 - 4302

Fax: 910 - 668 - 0101

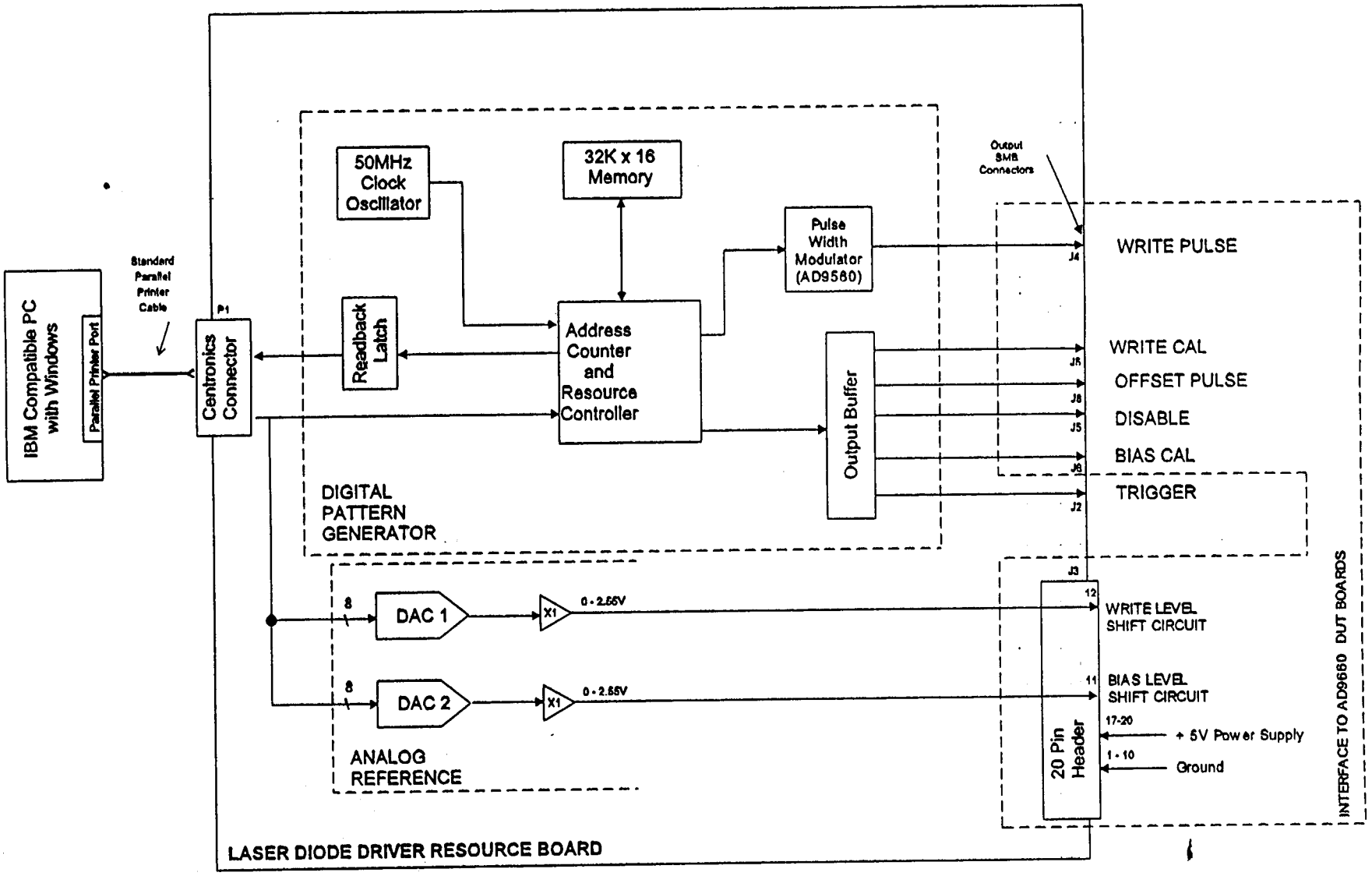
Our mailing address is:

Analog Devices
CPL Team
7910 Triad Center Drive
Greensboro, NC 27409

Attachments:

1. LDD Resource Board Block Diagram
2. MOD50.pat pattern description
3. MODMIX.pat pattern description
4. PCAL30.pat pattern description
5. PCAL20.pat pattern description
6. AD9660 DEMO DUT Board schematic, layout, bill of material
7. LDD Resource Board schematic, layout, bill of material

REV 2.0 2/23/96



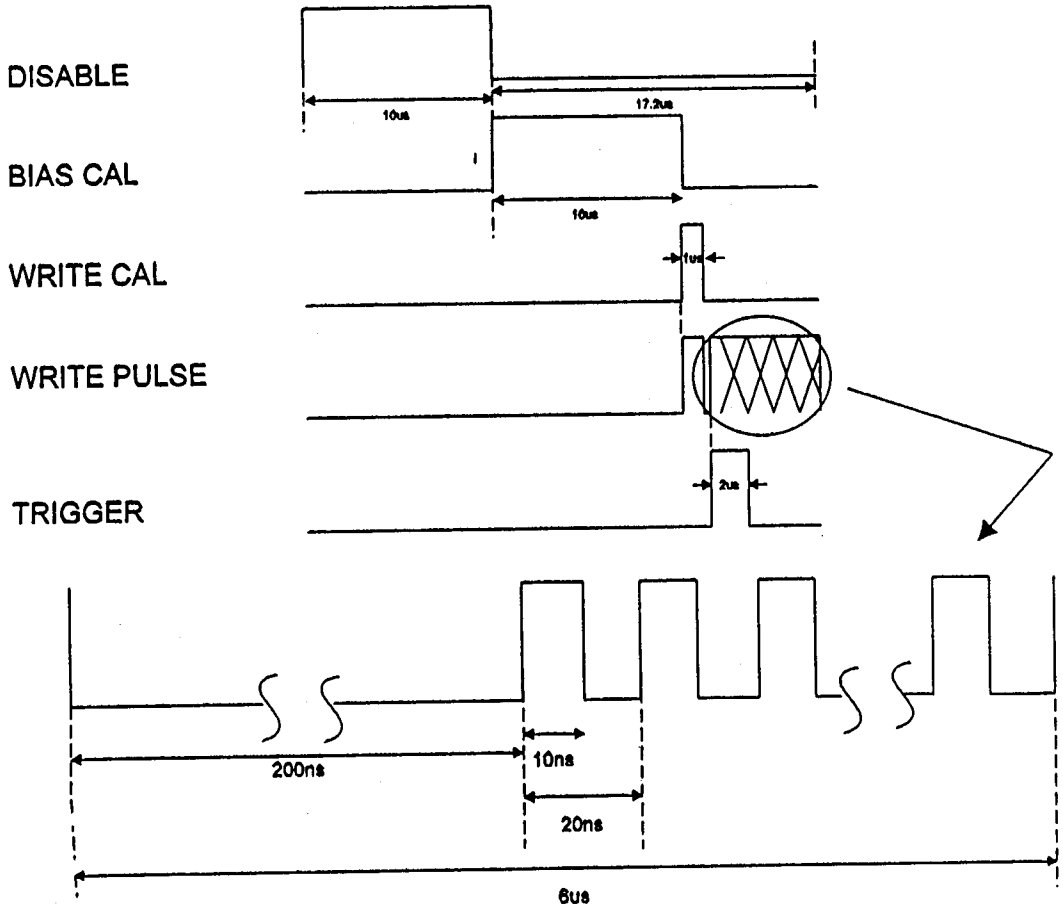
Laser Diode Driver Resource Board Block Diagram

Laser Diode Driver Resource Board Pattern Files

Pattern File: MOD50.PAT

Assumptions: CLOCK OSCILLATOR=50MHz, C_BIAS HOLD=1000pF, C_WRITE HOLD=100pF, OFFSET SET=NA

Notes: OFFSET PULSE not used. PWM mode is always Leading Edge Modulation.



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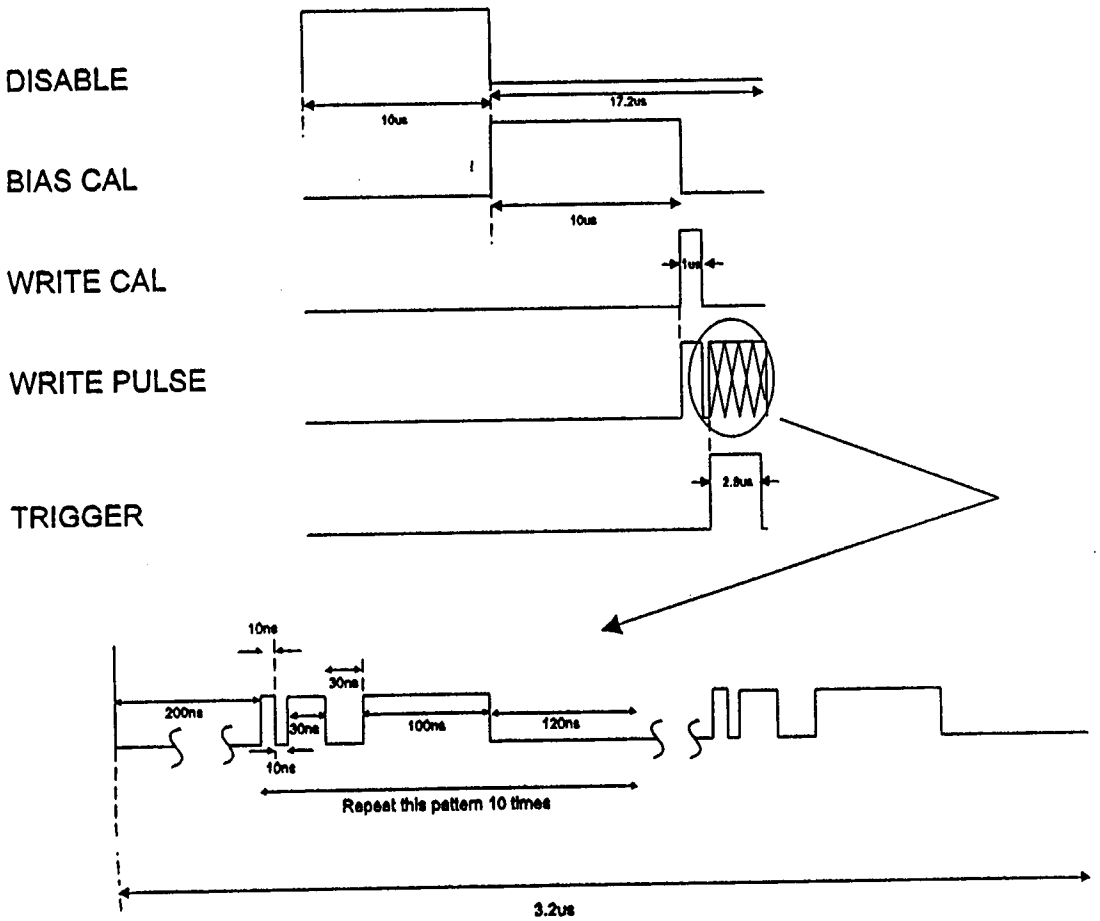
Laser Diode Driver Resource Board Pattern Files

Pattern File: MODMIX.PAT

Assumptions: CLOCK OSCILLATOR=50MHz, C_BIAS HOLD=1000pF, C_WRITE HOLD=100pF, OFFSET SET=NA

Notes: OFFSET PULSE not used. PWM mode is always Trailing Edge Modulation.



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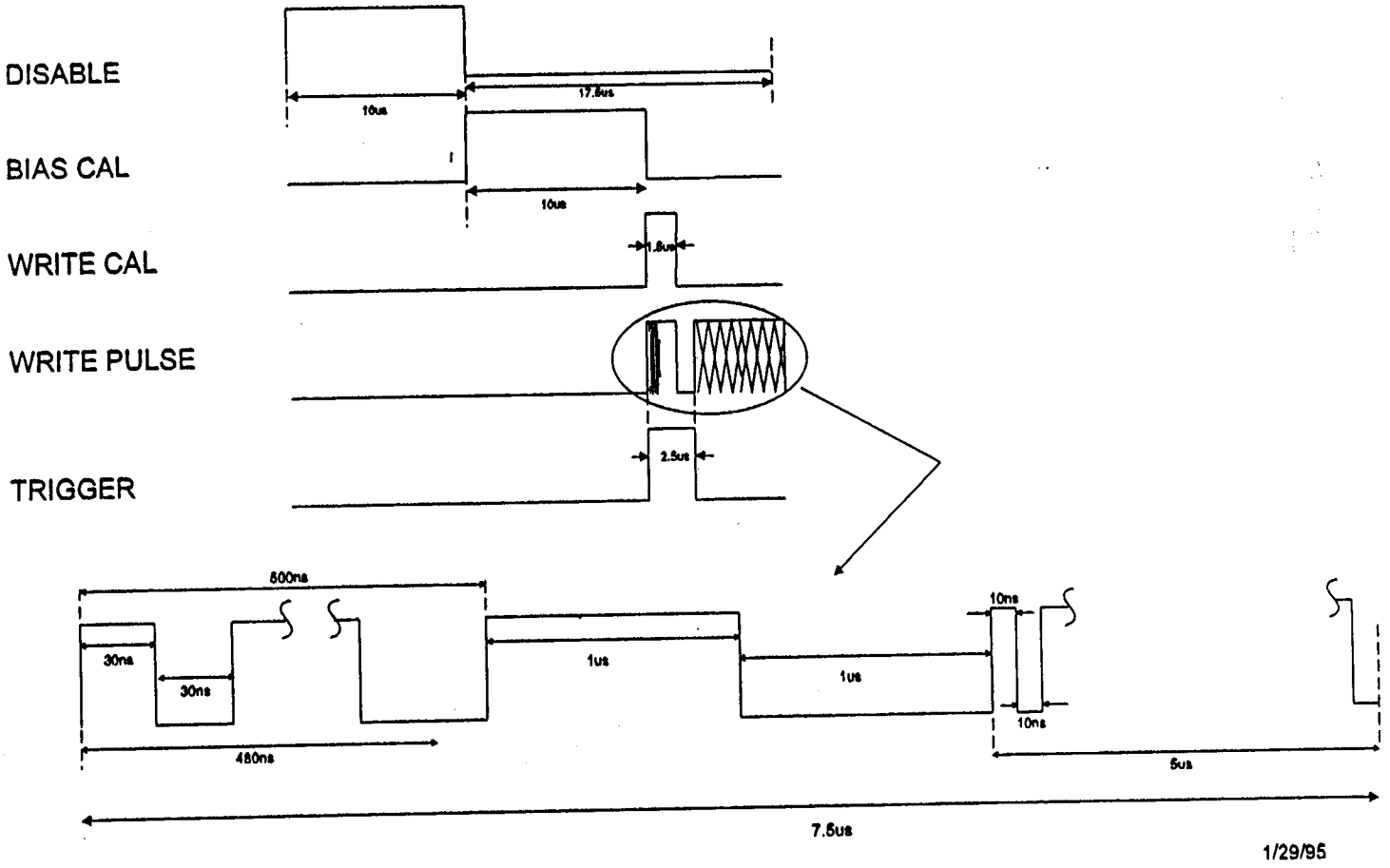
Laser Diode Driver Resource Board Pattern Files

Pattern File: PCAL30.PAT

Assumptions: CLOCK OSCILLATOR=50MHz, C_BIAS HOLD=1000pF, C_WRITE HOLD=100pF, OFFSET SET=NA

Notes: OFFSET PULSE not used. PWM mode is always Trailing Edge Modulation.

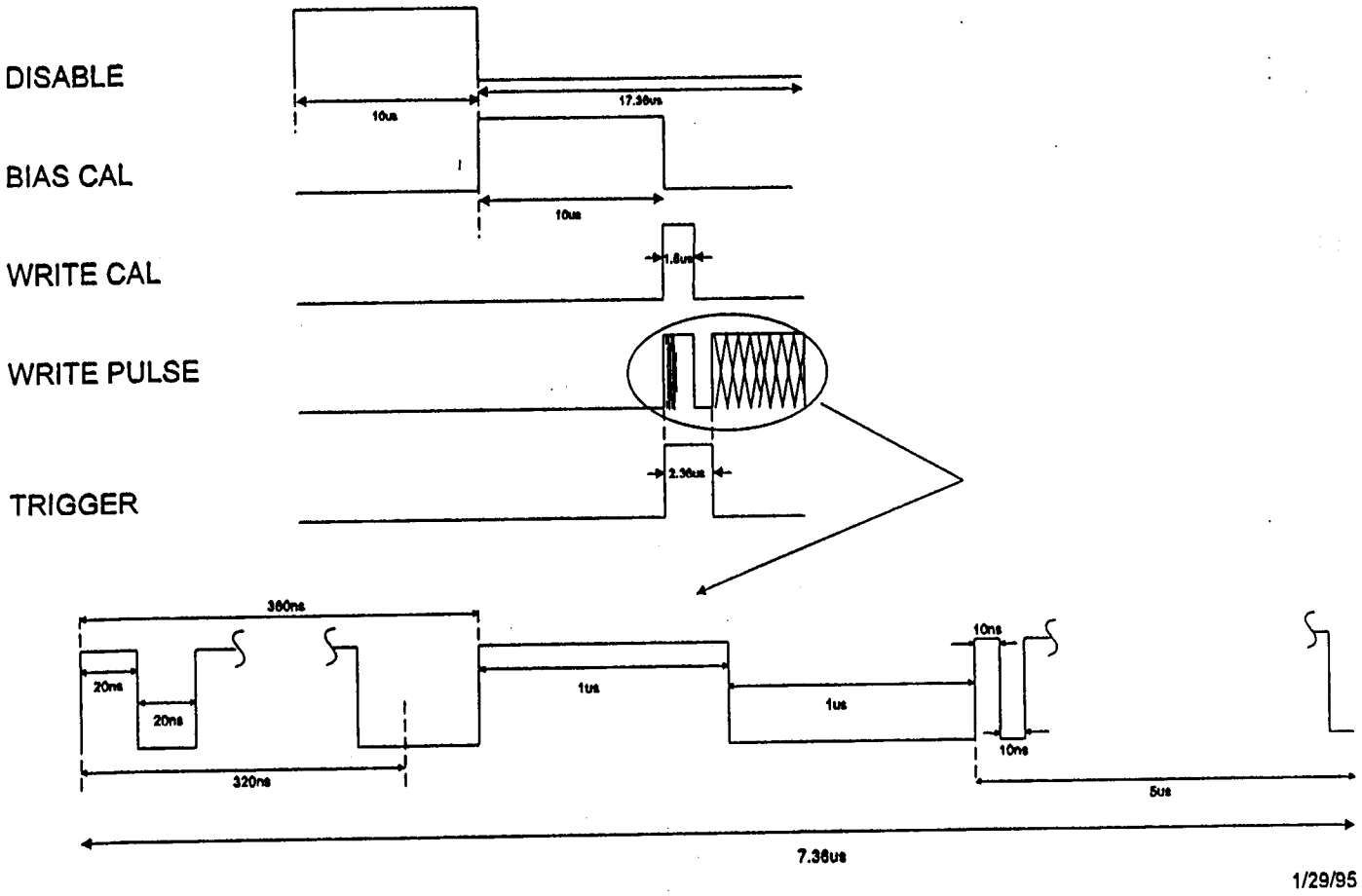


Laser Diode Driver Resource Board Pattern Files

Pattern File: PCAL20.PAT

Assumptions: CLOCK OSCILLATOR=50MHz, C_BIAS HOLD=1000pF, C_WRITE HOLD=100pF, OFFSET SET=NA

Notes: OFFSET PULSE not used. PWM mode is always Trailing Edge Modulation.



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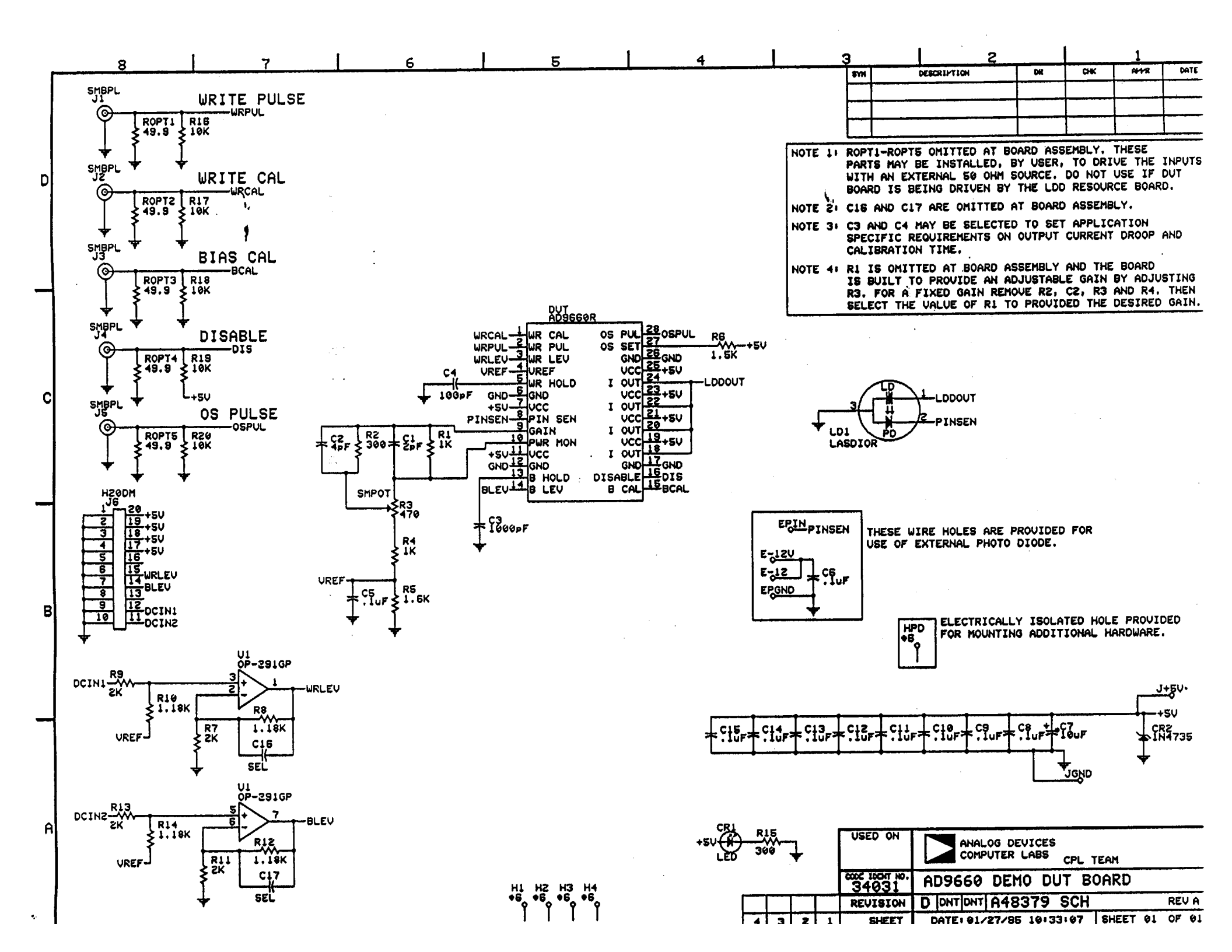


SYM	DESCRIPTION	DR	CHK	APVR	DATE

NOTE 1: ROPT1-ROPT5 OMITTED AT BOARD ASSEMBLY. THESE PARTS MAY BE INSTALLED, BY USER, TO DRIVE THE INPUTS WITH AN EXTERNAL 50 OHM SOURCE. DO NOT USE IF DUT BOARD IS BEING DRIVEN BY THE LDD RESOURCE BOARD.

NOTE 2: C16 AND C17 ARE OMITTED AT BOARD ASSEMBLY.

NOTE 3: C3 AND C4 MAY BE SELECTED TO SET APPLICATION SPECIFIC REQUIREMENTS ON OUTPUT CURRENT DROOP AND CALIBRATION TIME.

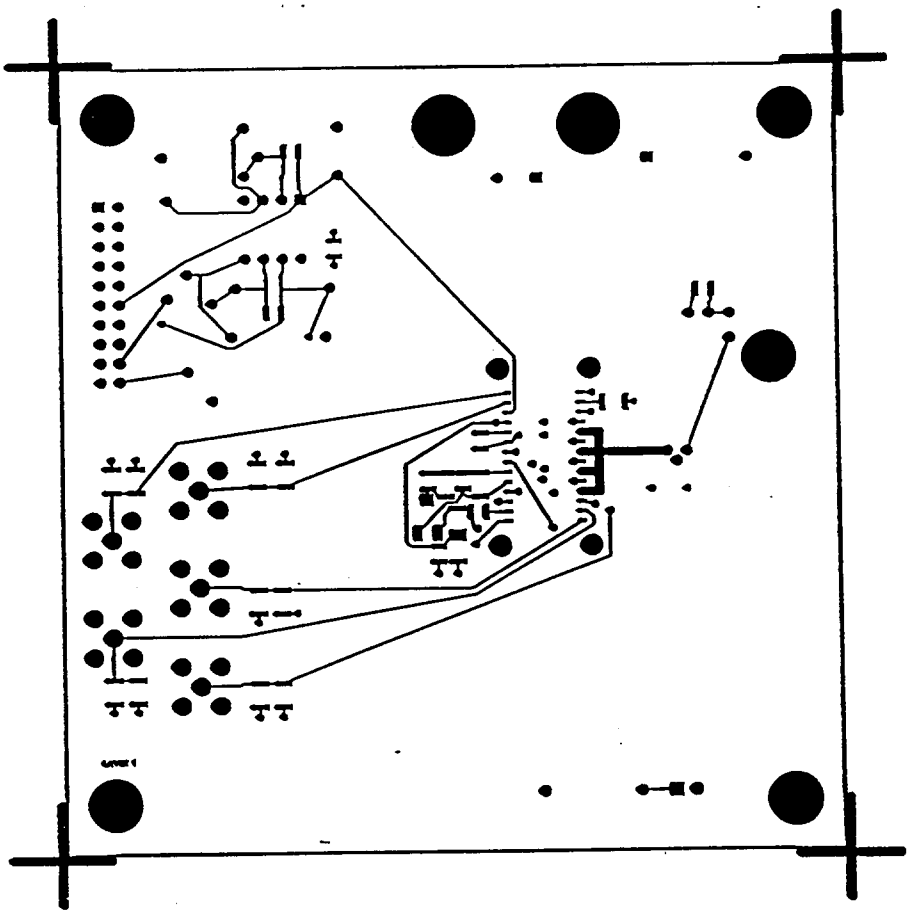
NOTE 4: R1 IS OMITTED AT BOARD ASSEMBLY AND THE BOARD IS BUILT TO PROVIDE AN ADJUSTABLE GAIN BY ADJUSTING R3. FOR A FIXED GAIN REMOVE R2, C2, R3 AND R4. THEN SELECT THE VALUE OF R1 TO PROVIDED THE DESIRED GAIN.

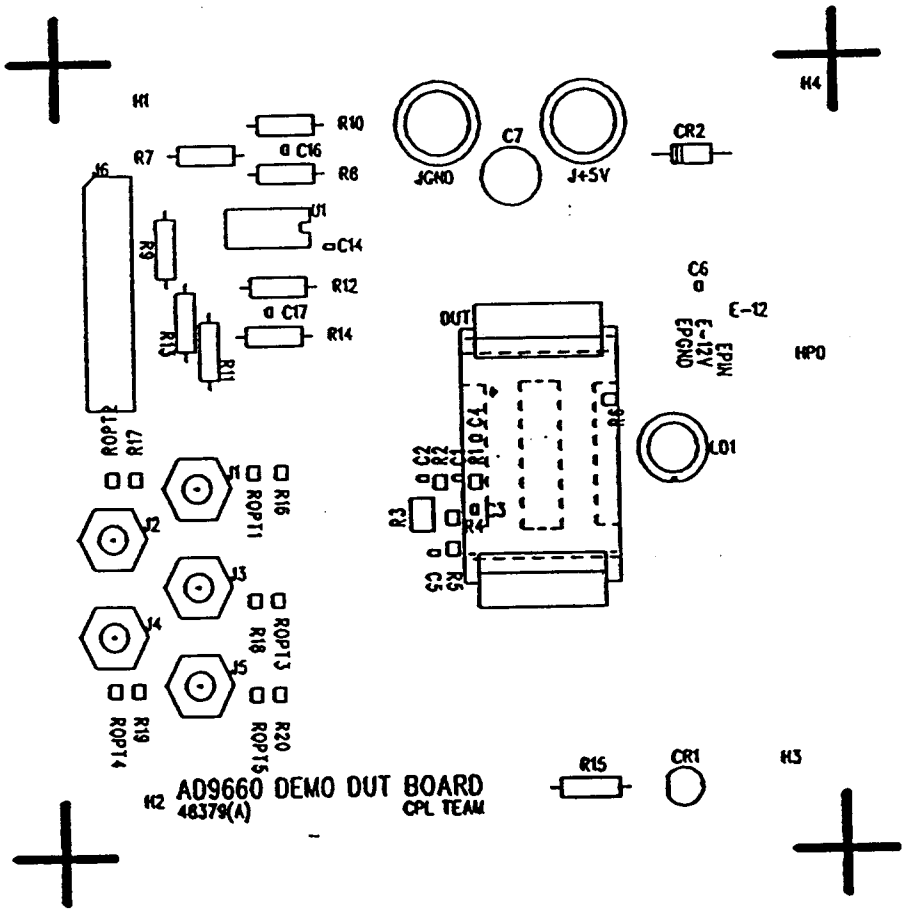
USED ON	ANALOG DEVICES COMPUTER LABS CPL TEAM
CODE IDENT NO. 34031	AD9660 DEMO DUT BOARD
REVISION	D DNT DNT A48379 SCH REV A
SHEET	DATE: 01/27/95 10:33:07 SHEET 01 OF 01

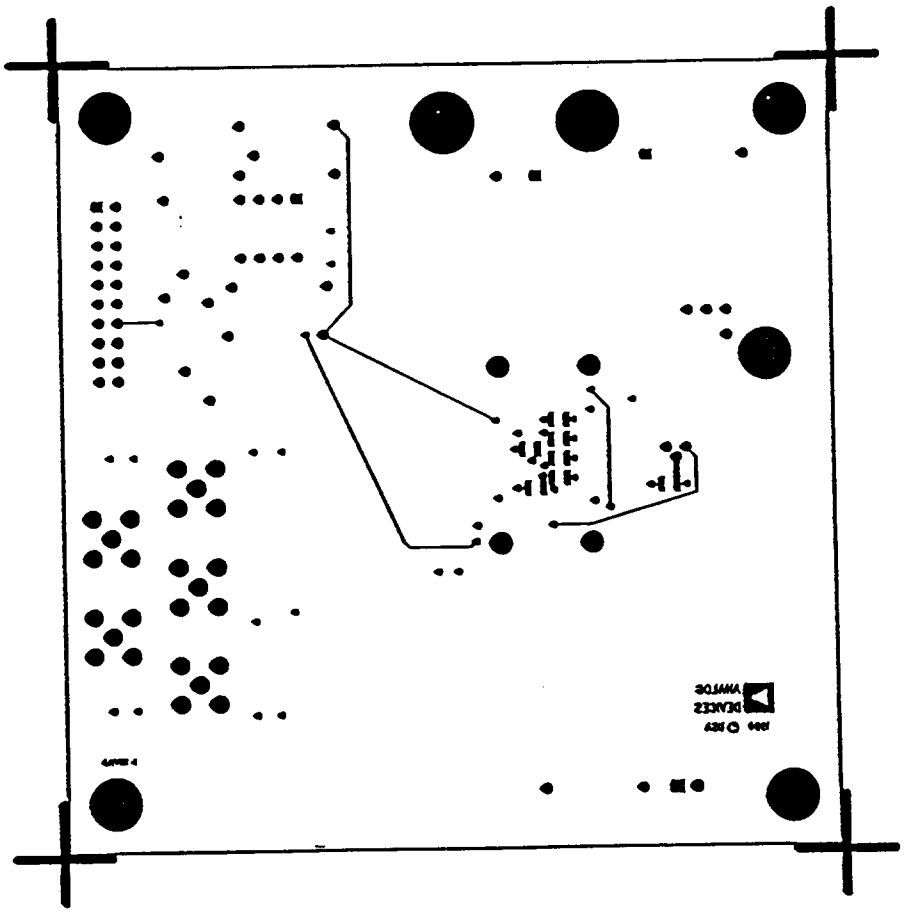
48379 REV. A AD9660 DEMO DUT BOARD FSCM NO. 34031 PAGE 1

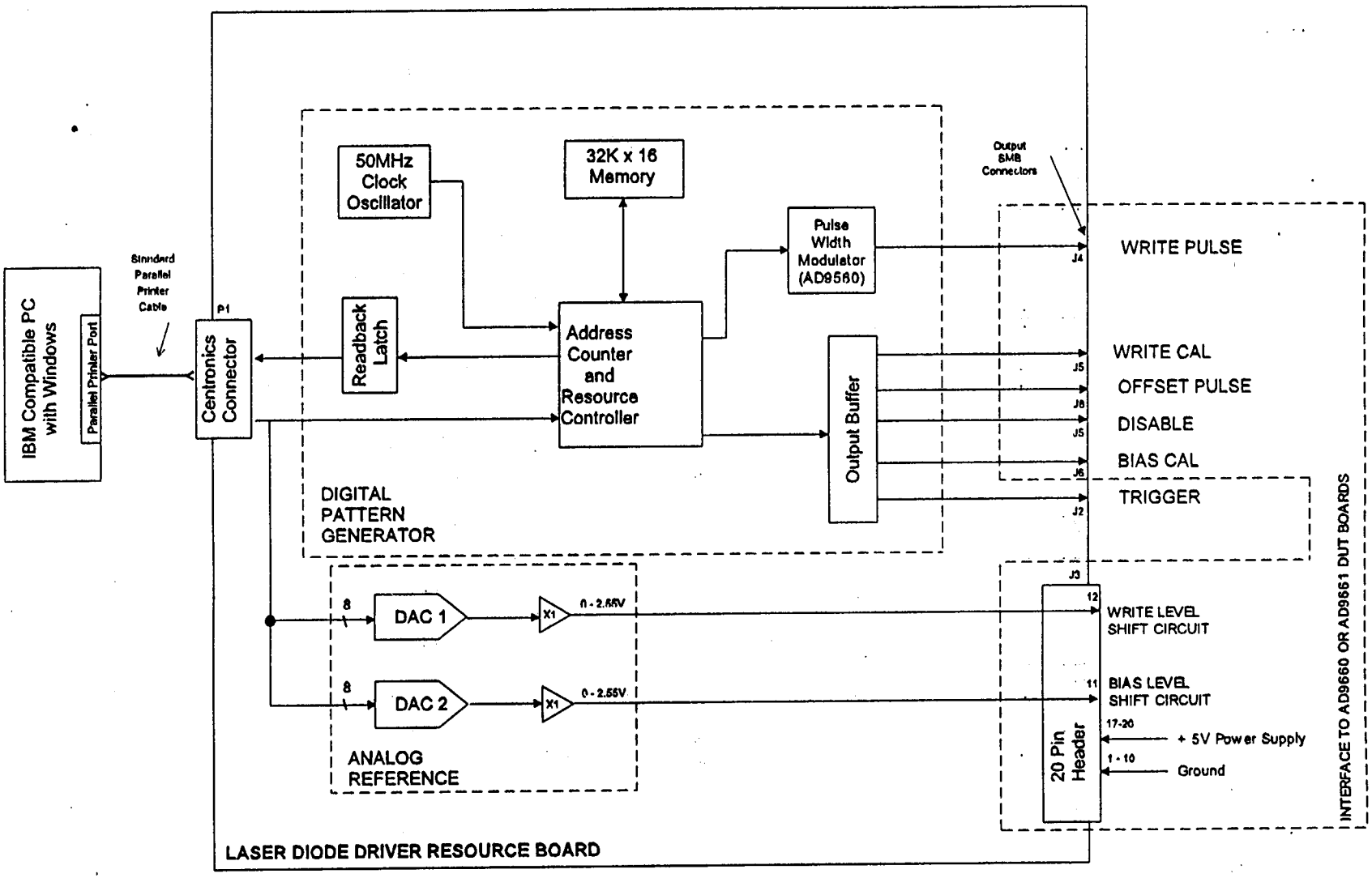
	QTY	STOCK NO.	REFD	DESCRIPTION
	5		H1,H2 H3,H4 HPD	#6 - #6 SCREW HOLE
	1		CR2	1N4735 - ZENER DIODE
	1		DUT	AD9660R - AD9660R DUAL LOOP LASER DIODE DRIVER
	10		C5,C6 C8,C9 C10, C11, C12, C13, C14, C15	BCAP0805 - CER CHIP CAP 0805,.1uF,,
5	1		C1	BCAP0805 - CER CHIP CAP 0805,2pF,,
6	1		C2	BCAP0805 - CER CHIP CAP 0805,4pF,,
7	4		C3,C4 C16, C17	BCAP0805 - CER CHIP CAP 0805,SEL,,
8	2		J+5V JGND	BJACK - BANANA JACK
9	1		R6	BRES1206 - SURF MT RES 1206,1.5K,,,
0	1		R5	BRES1206 - SURF MT RES 1206,1.6K,,,
1	5		R16, R17, R18, R19, R20	BRES1206 - SURF MT RES 1206,10K,,,
2	2		R1,R4	BRES1206 - SURF MT RES 1206,1K,,,
3	1		R2	BRES1206 - SURF MT RES 1206,300,,,
4	5		ROPT1 ROPT2 ROPT3 ROPT4 ROPT5	BRES1206 - SURF MT RES 1206,49.9,,,
5	1	3B08-291	J6	H20DM - HDR 20P DBL ROW MALE

QTY	STOCK NO.	REFD	DESCRIPTION
1		LD1	LASDIOR - LASER DIODE (LD: COM CATHODE/ PD: COM
1		CR1	LED - LIGHT EMITTING DIODE,
1		U1	OP-291GP - DIP RAIL-TO-RAIL OP-AMP
4		R8,R10 R12, R14	RC07 - RES CARBON,1.18K,,,
4		R7,R9 R11, R13	RC07 - RES CARBON,2K,,,
1		R15	RC07 - RES CARBON,300,,,
5		J1,J2 J3,J4 J5	SMBPL - SUBMIN SLIDE-ON (MALE) PCB MT PLUG
1		R3	SMPOT - SURFACE MOUNT POT ,470
1		C7	TAPC7 -TANT CAP,10uF,,,
4		E-12 EPIN E-12V EPGND	W-HOLE - WIRE HOLE

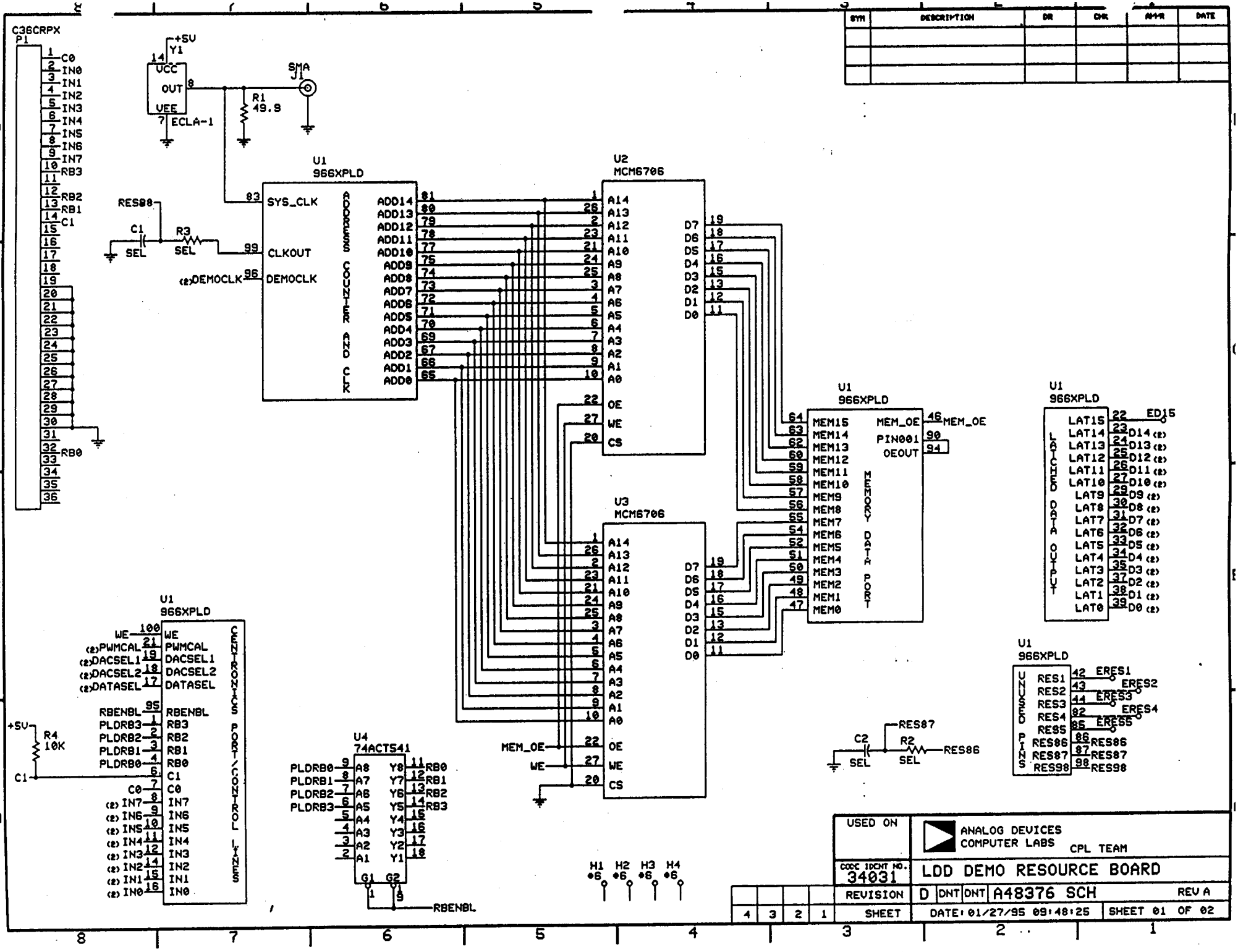



H1
H4
R10
R7
C16
R8
J6
U1
C14
R9
R12
C17
R13
R14
R11
ROPT
R17
J1
ROPT1
R16
J2
J3
ROPT3
R18
J4
J5
R19
ROPT4
ROPT5
R20
H2
AD9660 DEMO OUT BOARD
48379(A)
CPL TEAM
C7
JGND
J+5V
CR2
C6
E-12
EPWR
E-12V
EPGND
HP0
OUT
T3T1
R6
L01
C2
R2
C1
R1
R3
R4
J3
C5
R5
R15
CR1
H3





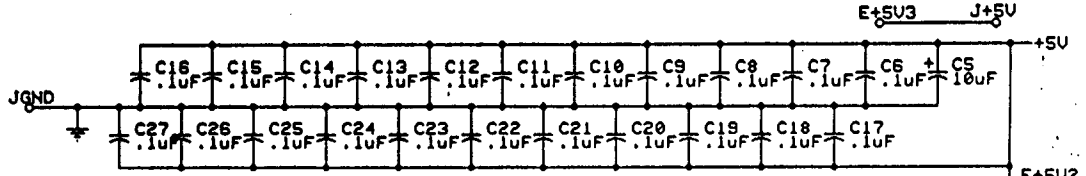
Laser Diode Driver Resource Board Block Diagram

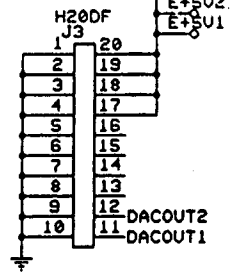


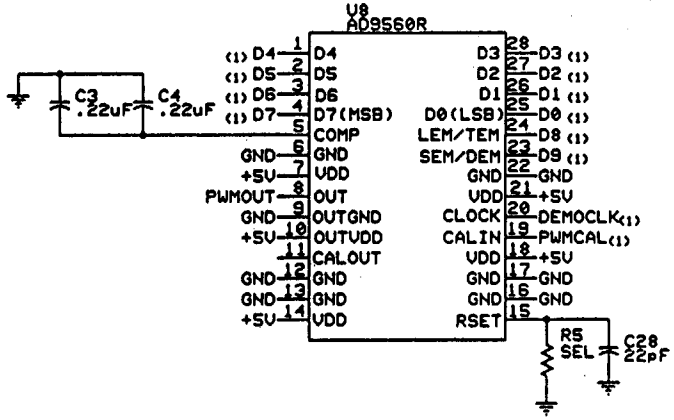
SYM	DESCRIPTION	BY	CHK	APVD	DATE

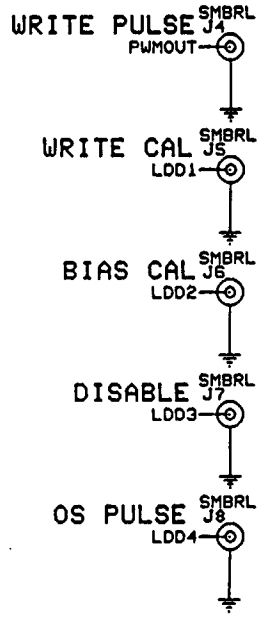
NOTE 1: C1, C2, R1, R2, R3, J1, J+5V AND JGND ARE OMITTED DURING BOARD ASSEMBLY.

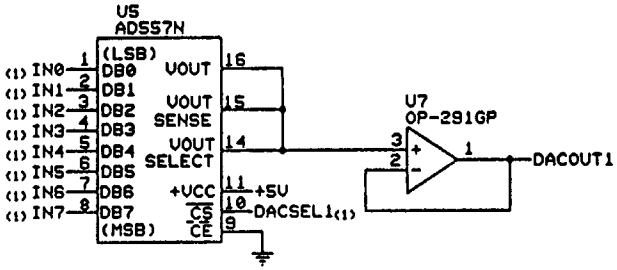
SYM	DESCRIPTION	DR	CHK	APVR	DATE

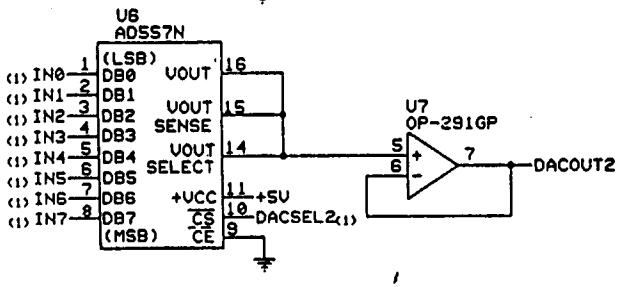


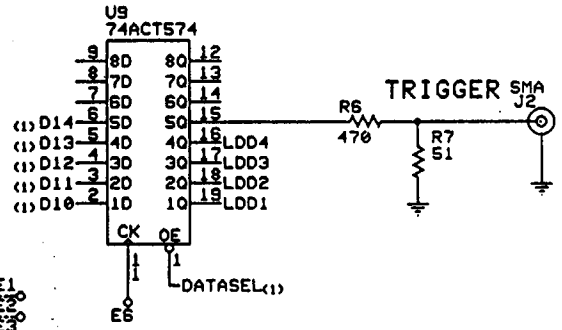


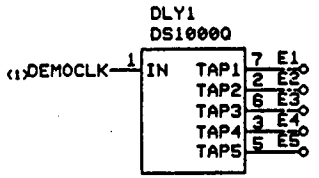










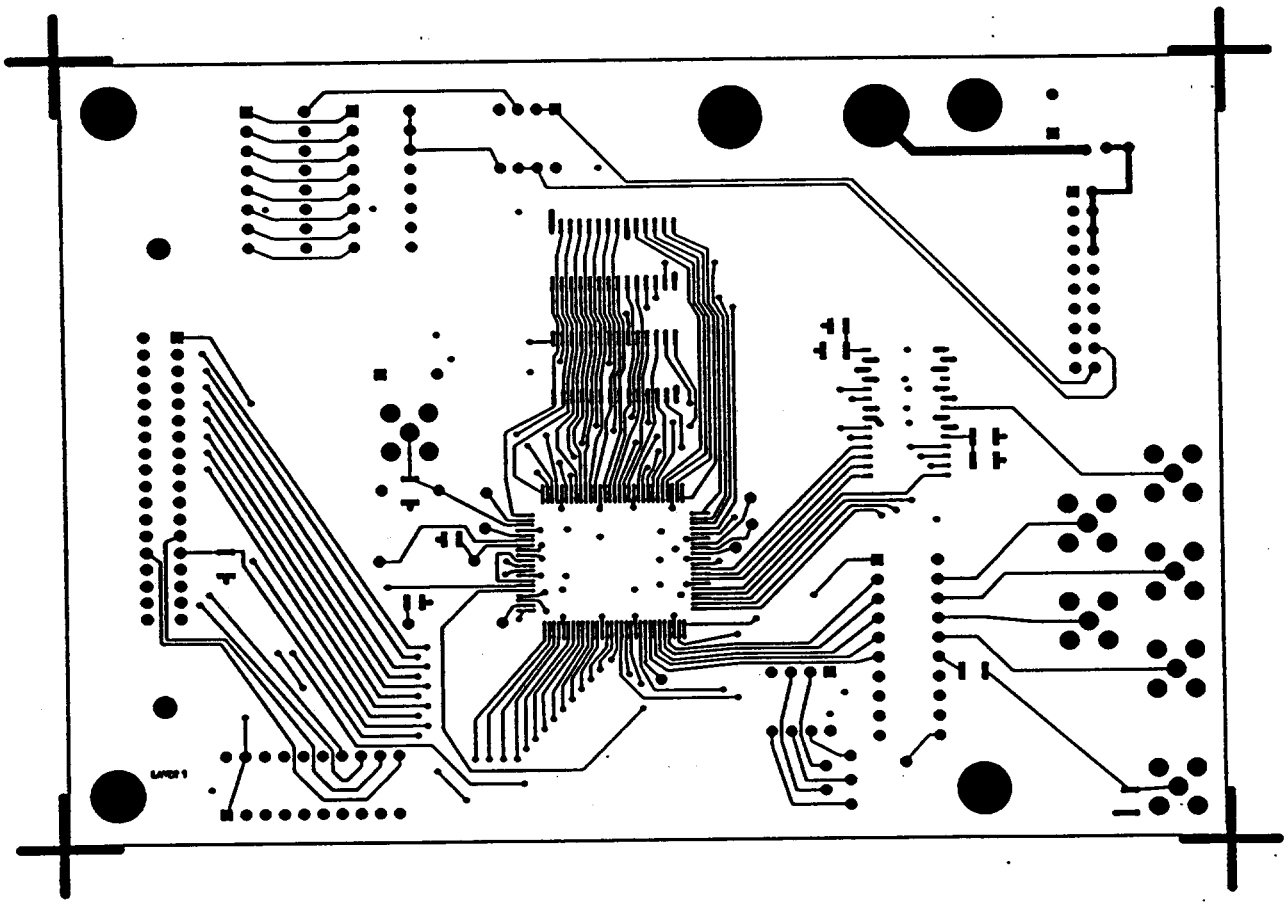


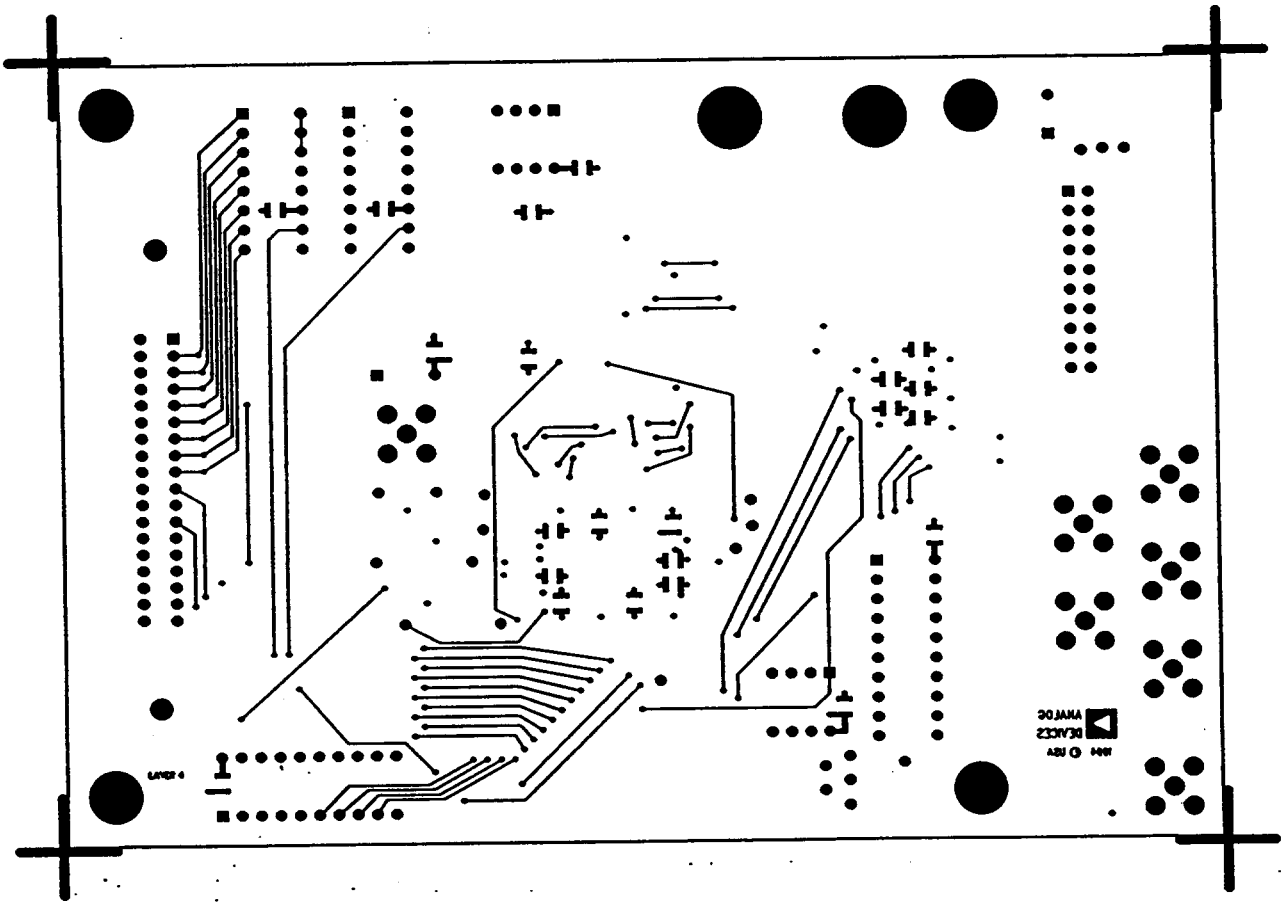
DS1000M-25 IS A DELAY LINE WITH A FULLSCALE DELAY OF 25nS. STRAPPED AT BOARD ASSEMBLY E3-E6 TO PROVIDE 15nS OF DELAY.

USED ON				ANALOG DEVICES COMPUTER LABS CPL TEAM	
CODE IDENT NO. 34031				LDD DEMO RESOURCE BOARD	
				REVISION	D DNT DNT A48376 SCH REV A
4	3	2	1	SHEET	DATE: 01/27/95 09:48:45 SHEET 02 OF 02

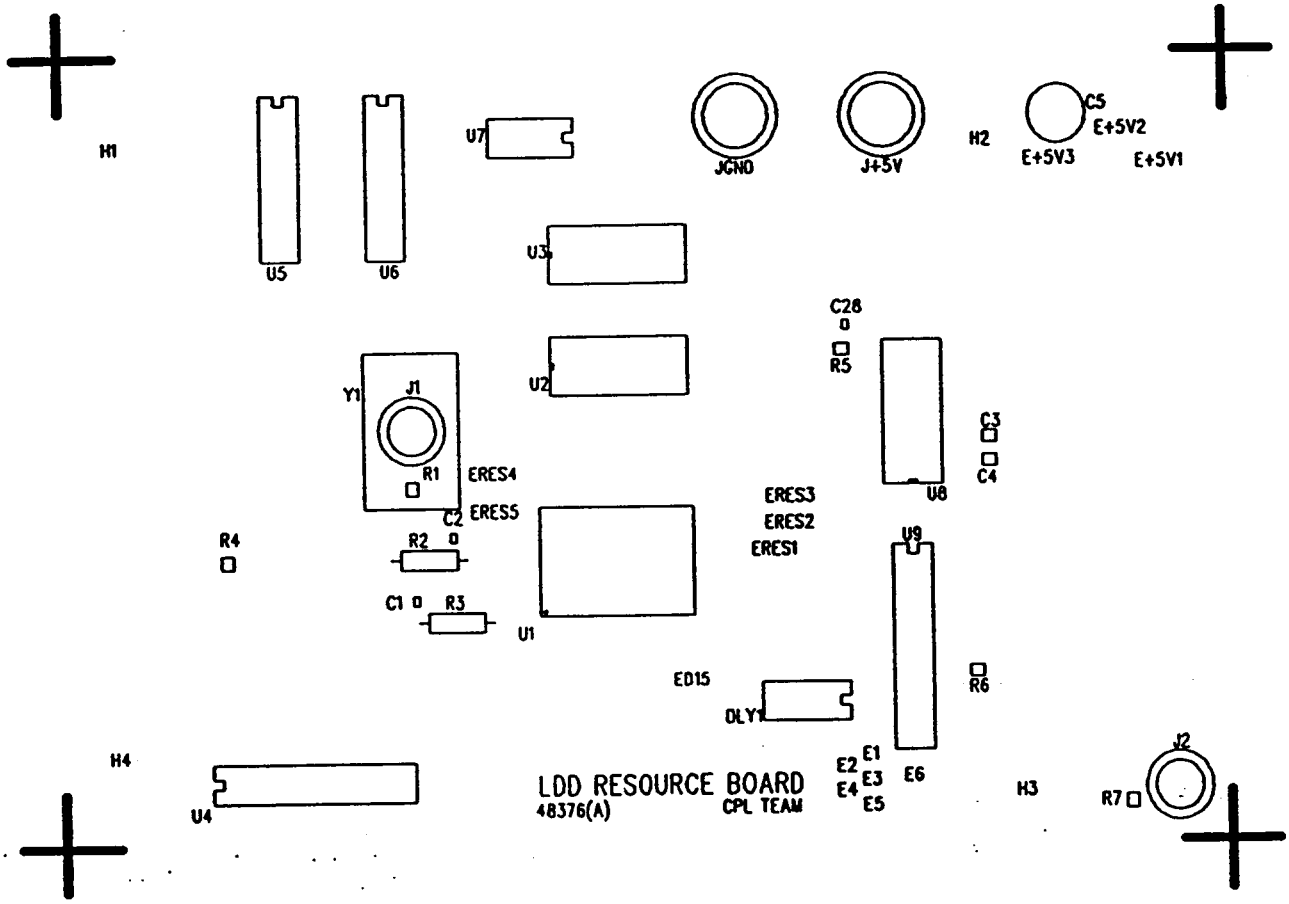
TEM	QTY	STOCK NO.	REFD	DESCRIPTION
1	4		H1,H2 H3,H4	#6 - #6 SCREW HOLE
2	1	0	U4	74ACT541 - ACT-TTL OCTAL BUFFER
3	1	300-0574-00	U9	74ACT574 - ACT-TTL OCTAL FLIP-FLOP
4	1		U1	966XPLD - LDD RESOUCE PLD
5	2	2A07-361	U5,U6	AD557N - DACPORT COMPATIBLE 8-BIT DAC
6	1		U8	AD9560R - PULSE WIDTH MODULATOR
7	22		C6,C7 C8,C9 C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27	BCAP0805 - CER CHIP CAP 0805,.1uF,,
8	1		C28	BCAP0805 - CER CHIP CAP 0805,22pF,,
9	2		C1,C2	BCAP0805 - CER CHIP CAP 0805,SEL,,
10	2		C3,C4	BCAP1206 - CER CHIP CAP 1206,.22uF,,
11	2		J+5V JGND	BJACK - BANANA JACK
12	1		R4	BRES1206 - SURF MT RES 1206,10K,,,
13	1		R6	BRES1206 - SURF MT RES 1206,470,,,
14	1		R1	BRES1206 - SURF MT RES 1206,49.9,,,

ITEM	QTY	STOCK NO.	REFD	DESCRIPTION
15	1		R7	BRES1206 - SURF MT RES 1206,51,,,
16	1		R5	BRES1206 - SURF MT RES 1206,SEL,,,
17	1	<P4)	P1	C36CRPX - 36P D CONN RT ANG PLSTC PCMT FEMALE
18	1		DLY1	DS1000Q - 5 TAP SILICON DELAY LINE,
19	1		Y1	ECLA-1 - XTAL CLK OSC,,,,
20	1	3B06-289	J3	H20DF - HDR 20P DBL ROW FEMALE
21	2		U2,U3	MCM6706 - 32K X 8 STATIC RAM
22	1		U7	OP-291GP - DIP RAIL-TO-RAIL OP-AMP
23	2		R2,R3	RC07 - RES CARBON,SEL,,,
24	2	3B15-300	J1,J2	SMA - SMA PCB MT
25	5	3D08-779	J4,J5 J6,J7 J8	SMBRL - SUBMIN SLIDE-ON (FEM) PCB MT RECP
26	1		C5	TAPC7 -TANT CAP,10uF,,,
27	15		E1,E2 E3,E4 E5,E6 ED15 E+5V1 E+5V2 E+5V3 ERES1 ERES2 ERES3 ERES4 ERES5	W-HOLE - WIRE HOLE





C23
C22
C21
C20
C19
C26
C16
C18
C14
C17
C15
C24
C25
C12
C10
C11
C8
C7
C6
C9
C27
P1
SL
J4
J5
J6
J2
J3


H1
U5
U6
U7
JGND
J+5V
H2
C5
E+5V2
E+5V3
E+5V1
U3
C28
R5
U2
Y1
J1
R1
ERES4
C2
ERES5
U8
C3
C4
ERES3
ERES2
ERES1
U9
R4
R2
C1
R3
U1
ED15
DLY1
R6
H4
U4
LDD RESOURCE BOARD
48376(A)
CPL TEAM
E1
E2
E3
E4
E5
E6
H3
J2
R7